Applied Physics Express

The Japan Society of Applied Physics

ACCEPTED MANUSCRIPT

Investigations of the gate-instability characteristics in Schottky/ohmic type p-GaN gate normally-off AlGaN/GaN HEMTs

To cite this article before publication: Changkun Zeng *et al* 2019 *Appl. Phys. Express* in press https://doi.org/10.7567/1882-0786/ab52cc

Investigations of the gate-instability characteristics in Schottky/ohmic type p-GaN gate normally-off AlGaN/GaN HEMTs

Changkun Zeng[1], Weizong Xu[1]*, Yuanyang Xia[2], Danfeng Pan[1], Yiwang Wang[1], Qiang Wang[2], Youhua Zhu[2,3], Fangfang Ren[1], Dong Zhou[1], Jiandong Ye[1], Dunjun Chen[1], Rong Zhang[1], Youdou Zheng[1], and Hai Lu[1]*

[1] *School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, China.*

[2] *CorEnergy Semiconductor Co. Ltd., Suzhou 215600, China*

[3] *School of Electronics and Information, Nantong University, Nantong 226019, China*

E-mail: wz.xu@nju.edu.cn, hailu@nju.edu.cn

In this work, the impacts of Schottky- and ohmic-type gate contacts on devices stability of p-GaN gate AlGaN/GaN high electron mobility transistors were experimentally investigated. In the Schottky-gate devices, drastic gate instability were observed under positive gate bias and elevated temperatures, featuring evident negative threshold voltage shift especially at low gate voltage region. By contrast, ohmic-gate devices exhibit superior gate stability with near-zero threshold voltage shift. Correspondingly, a physics picture of hole injection/emission processes in the p-GaN layer was established for the understanding of the distinct gate stability behaviors with different gate contact types.

Normally-off AlGaN/GaN high electron mobility transistors (HEMTs) have received increasing demands in power applications for their fail-safe operation capability and simple gate drive configuration.[1-2)] Among the approaches to realize intrinsic normally-off operation, p-GaN gate technology, which employs a p-GaN cap layer to deplete the 2-dimensional electron gas (2DEG) channel, has dominated the scene of commercialization owing to its lower parasitic inductance and advantageous $R_{ON} \cdot Q_G$ figure of merit.[3-4)] Meanwhile, high speed and high efficiency GaN power integrated circuits based on p-GaN gate power HEMTs have also been demonstrated in recent years.[5-6)]

The gate structure of metal/p-GaN/AlGaN/GaN consists of a hetero p-i-n junction and a metal/p-GaN junction of either Schottky or ohmic type.[7-8)] As compared to an ohmic-type gate, the Schottky gate contact features lower gate leakage current and larger gate driving margin, given that the metal/p-GaN Schottky junction is reverse biased at a forward gate bias.[4,9-10)] However, due to the poor blocking capability of the Schottky junction on the Mg doped p-GaN layer,[11-13)] hole injection occurs under the forward gate bias.[13-14)] These extra holes in the gate stacks could then cause unfavorable gate instability issues.[8,15-16)] The resultant threshold voltage (V_{th}) shift may induce unintentional operation point drift of the device that causes extra power conversion efficiency loss or gate degradation.[17-20)] Therefore, to further optimize the gate contact structure for the p-GaN gate normally-off AlGaN/GaN HEMT, it is of particular interest to make clear the gate stability characteristics and to clarify the underlying physical mechanism of possible gate instability for both Schottky/ohmic-type gated devices.

In this work, p-GaN gate AlGaN/GaN HEMTs utilizing both Schottky and ohmic type gate contacts were demonstrated with their unique gate stability performances revealed. It was found that, Schottky-type p-GaN gate HEMT encounters evident gate instability under positive gate bias and elevated temperatures. And the shift of threshold voltage tends to be much higher in low gate voltage (V_{GS}) region, i.e. V_{GS} from 0 V to 3 V. A physics model of hole injection and accumulation in the floating p-GaN layer was established to understand these unique gate stability behaviors. In contrast, ohmic-type device exhibits excellent gate stability against gate bias and operation temperatures, which should be attributed to the conductive gate contact that effectively alleviates the hole accumulation effect.

Fig. 1(a) illustrates the cross-sectional schematic of the p-GaN gated AlGaN/GaN HEMTs. The epitaxial layer was grown by metal organic chemical vapor deposition (MOCVD) on a 6-inch commercial Si substrate. It consists of a 4.6-μm GaN buffer layer, a 300-nm GaN channel layer, a 1-nm AlN space layer, a 20-nm $Al_{0.17}Ga_{0.83}N$ barrier layer, and a 100-nm Mg-doped p-GaN cap layer. The Mg atom concentration in the p-GaN cap layer is 2×10^{19} cm^{-3}, and the hole density was measured to be 4.5×10^{17} cm^{-3} by Hall measurements.

In the device fabrication processes, device isolation was firstly performed with nitrogen ion implantation. Then, inductively coupled plasma (ICP) dry etching was utilized to etch the p-GaN in the ohmic region, and was followed by the treatment with Tetramethylammonium Hydroxide (TMAH) solution to remove the etching-related damages. Subsequently, metal stack of Ti/Al/Ni/Au (40/80/40/100 nm) was deposited for ohmic drain/source formation. Two types of gate contact for p-GaN gate HEMTs have been fabricated, i.e. Schottky and ohmic. Both contacts were made of Ni/Au (20/20 nm), while an extra 5-min post-annealing process at 550 °C in air (N_2:O_2 = 4:1) has been performed for the ohmic gate contact formation.[21-22] Fig. 1(b) illustrates the gate-to-gate *I-V* characteristics of both two types of gate contacts. The annealed gate contacts present near ohmic performance (red curve) and much higher current level in comparison to the as-deposited Schottky-type gate contacts (blue curve).

Static electrical characterization was firstly performed on the Schottky type gate contact devices with devices geometries of L_{GS}=6μm, L_G/W_G=4μm/90μm, L_{GD}=15μm. Fig. 1(c) presents the transfer gate leakage characteristics of the fabricated devices with a drain voltage (V_{DS}) of 0.5 V. The fabricated AlGaN/GaN HEMT exhibits a V_{th} of ~1.5 V by linear extraction, an on-to-off ratio up to 1×10^7 (red curves), a subthreshold swing (*SS*) of ~197 mV/dec, revealing the normally-off operation mode with excellent gate controllability.

Bi-directional *I-V* measurements were subsequently performed to evaluate the devices gate stability performances. As shown in Fig. 2(a), evident hysteresis in the transfer characteristics could be observed, featuring an elevated drain current (I_D) and negative V_{th} shift (ΔV_{th}) in the backward measuring curve. Fig. 2(b) plots the *I-V* characteristics of bi-directional measurements with various maximum forward gate bias (V_{GS_max}). With an

increasing V_{GS_max}, higher I_D and larger ΔV_{th} could be observed in the range of 0V < V_{GS_max} < 3V. This has revealed the dominance of positive gate bias in generating the observed gate instability. However, it should be noted that as the V_{GS_max} extends 3 V, ΔV_{th} and I_D exhibits saturation in the backward measurement.

These distinct behaviors observed in the bi-directional measurements should be attributed to the charge storage in the floating p-GaN layer.[23-24] Fig. 3 illustrates the energy band diagram of the gate stack of the p-GaN gate HEMT under different gate bias conditions. With a relatively low gate bias (0V < V_{GS} < 3V), the holes could be injected from the gate metal to the p-GaN layer either by tunneling through the Schottky junction barrier or by thermal emission, i.e. process (*i*) as illustrated in Fig. 3(a). Meanwhile, due to the band offset between the valence bands of p-GaN and AlGaN, the injected holes would accumulate at the p-GaN/AlGaN interface without leaking through the AlGaN barrier. Then, the p-GaN layer turns into a floating layer with extra positive charges, inducing downward band bending of gate stack and enhancing the accumulation of electrons in the 2DEG channel. Resultantly, increasing of I_D and negative shift of V_{th} could be observed. Under a higher gate bias (e.g., V_G > 3 V), the overall band bending of the hetero p-i-n junction would lead both the conduction and valence band of p-GaN layer become lower than that of the GaN channel, as illustrated in Fig. 3(b). Consequently, processes of 2DEG electrons spilling over the AlGaN barrier and pumping out of holes from p-GaN/AlGaN interface to the GaN channel would be triggered,[25] contributing to a sharp increase of gate leakage. This was verified by the measured I_G characteristics at V_{GS} > 3 V, as presented in Fig. 1(c). Both these two processes would counteract the holes accumulation at p-GaN/AlGaN interface either by electron-holes recombination or by directly pumping out the holes, in spite of enhanced hole injection from the gate metal at higher forward gate bias.[8] Ultimately, gate instability as a result of extra holes accumulated at p-GaN/AlGaN interface would be alleviated, as shown in Fig. 2.

In the backward measurement, as the gate bias drops to near zero in the backward *I-V* measurement, i.e. the knee point B in Fig. 2(a), the blocking effect of Schottky junction barrier on the accumulated holes reduces. This would facilitate the release of holes from the p-GaN/AlGaN interface to gate metal, i.e. process (*iv*) as illustrated in Fig. 3(c). The

gate-bias-driving removal of the extra holes in the gate stack would contribute an extra negative variation of V_{GS} (ΔV_{GS}), resulting in a reduced *SS*.[26] This process was verified by the sub-60mV/dec *SS*, i.e. 54 mV/dec, being apparently lower than those of previously reported p-GaN gate AlGaN/GaN HEMTs.[27-28]

Presented in Fig. 4 are the temperature dependent transfer curves from bi-directional measurements. As temperature increased from 25 ˚C to 125 ˚C, V_{th} shifted negatively in the forward measurements, thus temperature dependent gate instability was verified. This could be explained by the enhanced hole injection from the gate metal to the floating p-GaN layer via thermal assisted emissions. The resultant larger number of accumulated holes from the gate metal would induce higher positive charging effect in the gate stack and thus lead to lower V_{th}. It could be noted that the on-state I_{DS} drops with the elevated temperature, which should be a result of the mobility degradation in the 2DEG channel, being verified by the power law exponents of ~ -2.1 in the log-log fittings between I_D and the temperature at V_{GS} = 5 V.[29-31] The difference from the expected value of -1.5 for pure mobility degradation should be related to the temperature dependence of the access resistance.

As temperature went higher, processes of channel electrons spilling over the AlGaN barrier and holes injection into the GaN channel layer would be intensified and occur at lower gate bias. The negative shift in turning on voltage of I_G and point A at higher temperatures has validated this physics picture. On the other hand, only slight temperature dependence could be observed in the reverse measuring curve. This corresponds well with the physics model presented in Fig. 3(c), where the pumping of accumulated holes from p-GaN to the gate metal as gate bias dropped to negative should be dominated by the electric-field induced depletion, instead of thermal emission. In general, Schottky type p-GaN gate AlGaN/GaN HEMT is facing with serious intrinsic gate stability issues, being highly sensitive to forward gate bias (especially in low voltage range) and operation temperature.

As a comparison, transfer and gate stability characteristics of ohmic-type p-GaN gate AlGaN/GaN HEMT have been evaluated with results presented in Fig. 5(a), where a comparatively lower V_{th} of ~ 0.35 V is exhibited. And in the bi-directional measurements,

nearly zero hysteresis could be observed in the transfer characteristics, independent of forward gate bias and measuring temperature. This should be attributed to the absence of the floating p-GaN region between the Schottky junction barrier and the p-GaN/AlGaN interface. Therefore, in terms of gate stability, ohmic-type p-GaN gate AlGaN/GaN HEMT features more desirable gate stability against both gate forward bias and temperature.

In summary, this work has focused on the impacts of Schottky and ohmic gate contact on gate stability performances of p-GaN gate AlGaN/GaN HEMTs. It was found that, devices with Schottky-type gate contact are facing with serious intrinsic gate stability issues, being sensitive to positive gate bias and operation temperatures, especially in low positive gate bias region, while ohmic-gate devices exhibited excellent stability against gate bias and operation temperature. These findings are believed to provide substantial knowledge for further optimizing the gate contact structure of p-GaN gate AlGaN/GaN HEMTs, e.g. a hybrid combination of Schottky and ohmic gate contact structure might be promising in obtaining the balance between gate control capability and stability in the power applications.

Acknowledgement

This work was supported by the National Key R&D Program of China (No. 2017YFB0403000).

References

1) H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P. R. Chalker, M. Charles, K. J. Chen, N. Chowdhury, R. Chu, C. De Santi, M. M. De Souza, S. Decoutere, L. Di Cioccio, B. Eckardt, T. Egawa, P. Fay, J. J. Freedsman, L. Guido, O. Häberlen, G. Haynes, T. Heckel, D. Hemakumara, P. Houston, J. Hu, M. Hua, Q. Huang, A. Huang, S. Jiang, H. Kawai, D. Kinzer, M. Kuball, A. Kumar, K. B. Lee, X. Li, D. Marcon, M. März, R. McCarthy, G. Meneghesso, M. Meneghini, E. Morvan, A. Nakajima, E. M. S. Narayanan, S. Oliver, T. Palacios, D. Piedra, M. Plissonnier, R. Reddy, M. Sun, I. Thayne, A. Torres, N. Trivellin, V. Unni, M. J. Uren, M. Van Hove, D. J. Wallis, J. Wang, J. Xie, S. Yagi, S. Yang, C. Youtsey, R. Yu, E. Zanoni, S. Zeltner, and Y. Zhang, J. Phys. D, Appl. Phys. **51**, 163001 (2018).
2) K. J. Chen, O. Häberlen, A. Lidow, C. lin Tsai, T. Ueda, Y. Uemoto, and Y. Wu, IEEE Transactions on Electron Devices **64**, 779 (2017).
3) O. Hilt, F. Brunner, E. Cho, A. Knauer, E. Bahat-Treidel, and J. Würfl, IEEE 23rd International Symposium on Power Semiconductor Devices and ICs 239 (2011).
4) I. Hwang, J. Kim, H. S., Choi, H., Choi, J., Lee, K. Y. Kim, J. Park, J. C. Lee, J. Ha, J. Oh, J. Shin, and U. Chung, IEEE Electron Device Letters **34**, 202 (2013).
5) T. J. Flack, B. N. Pushpakaran, and S. B. Bayne, Journal of Electronic Materials **45**, 2673 (2016).
6) E. A. Jones, F. F. Wang, and D. Costinett, IEEE Journal of Emerging and Selected Topics in Power Electronics **4**, 707 (2016).
7) B. Li, H. Li, J. Wang, and X. Tang, IEEE Electron Device Letters **40**, 1389 (2019).
8) J. He, G. Tang, and K. J. Chen, IEEE Electron Device Letters **39**, 1576 (2018).
9) F. Lee, L. Y. Su, C. H. Wang, Y. R. Wu, and J. Huang, IEEE Electron Device Letters **36**, 232 (2015).
10) L. Efthymiou, G. Longobardi, G. Camuso, T. Chien, M. Chen, and F. Udrea, Applied Physics Letters **110**, 123502 (2017).
11) K. Shiojima, T. Sugahara, and S. Sakai, Applied Physics Letters **77**, 4353 (2000).
12) M. ˇTapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmík, IEEE Electron Device Letters **37**, 385 (2016).
13) T. F. Chang, T. C. Hsiao, C. F. Huang, W. H. Kuo, S. F. Lin, G. S. Samudra, and Y. C.

Liang, IEEE Transactions on Electron Devices **62**, 339 (2014).

14) T. F. Chang, T. C. Hsiao, S. H. Huang, C. F. Huang, Y. H. Wang, G. S. Samudra, and Y. C. Liang, IEEE 11th International Conference on Power Electronics and Drive Systems 681 (2015).
15) J. Wei, R. Xie, H. Xu, H. Wang, Y. Wang, M. Hua, K. Zhong, G. Tang, J. He, M. Zhang, and K. J. Chen, IEEE Electron Device Letters **40**, 526 (2019).
16) H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, IEEE Trans. Power Electron. **32**, 5539 (2017).
17) A. N. Tallarico, S. Stoffels, N. Posthuma, P. Magnone, D. Marcon, S. Decoutere, E. Sangiorgi, and C. Fiegna, IEEE Transactions on Electron Devices **65**, 38 (2017).
18) I. Rossetto, M. Meneghini, F. Canato, M. Barbato, S. Stoffels, N. Posthuma, S. Decoutere, A. N. Tallarico, G. Meneghesso, and E. Zanoni, Microelectronics Reliability **76**, 298 (2017).
19) E. Zanoni, M. Meneghini, G. Meneghesso, D. Bisi, I. Rossetto, and A. Stocco, IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications 75 (2015).
20) X. Li, G. Xie, C. Tang, and K. Sheng, Microelectronics Reliability **65**, 35 (2016).
21) J. Chen, W. D. Brewer, Advanced Electronic Materials **1**, 1500113 (2015).
22) B. Sarkar, P. Reddy, A. Klump, F. Kaess, R. Rounds, R. Kirste, S. Mita, E. Kohn, R. Collazo, and Z. Sitar, Journal of Electronic Materials **47**, 305 (2018).
23) M. Ruzzarin, M. Meneghini, A. Barbato, V. Padovan, O. Haeberlen, M. Silvestri, T. Detzel, G. Meneghesso, and E. Zanoni, IEEE Transactions on Electron Devices **65**, 2778 (2018).
24) A. Stockman, F. Masin, M. Meneghini, E. Zanoni, G. Meneghesso, B. Bakeroot, and P. Moens, IEEE Transactions on Electron Devices **65**, 5365 (2018).
25) X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, IEEE Electron Device Letters **39**, 1145 (2018).
26) Y. Shi, Q. Zhou, Q. Cheng, P. Wei, L. Zhu, D. Wei, A. Zhang, Wanjun Chen, and B. Zhang, IEEE 30th International Symposium on Power Semiconductor Devices and ICs 96 (2018).
27) L. Y. Su, F. Lee, and J. J. Huang, IEEE Transactions on Electron Devices **61**, 460 (2014).

28) H. C. Chiu, Y. S. Chang, B. H. Li, H. C. Wang, H. L. Kao, C.W. Hu, and R. Xuan, IEEE Journal of the Electron Devices Society **6**, 201 (2018).

29) W. Tan, M. Uren, P. Fry, P. Houston, R. Balmer , and T. Martin, Solid-State Electron **50**, 511 (2006).

30) R. Wang, Y. Cai, K. J. Chen, Solid-state Electronics **53**, 1 (2009).

31) O. Hilt, E. Bahat-Treidel, F. Brunner, A. Knauer, R. Zhytnytska, P. Kotara, and J. Wuerfl, Journal of Physics: Conference Series **494**, 012001 (2014).

Figure Captions

Fig. 1. (a) Schematic cross-section image, (b) gate-to-gate *I*-*V* characteristics of both two types of gate contacts, (c) transfer and gate leakage characteristics at room temperature, of the p-GaN gate HEMT with Schottky-type gate contact.

Fig. 2. Transfer characteristics of p-GaN gate HEMT with Schottky-type gate contact in bi-directional measurements (a), and with different gate voltage sweeping range (b). The inset is the equivalent circuit of the p-GaN gate stack.

Fig. 3. Schematic band diagrams of the Schottky-metal/p-GaN/AlGaN/GaN structure under different gate bias conditions. The physical processes of hole/electron injections and recombination are illustrated schematically.

Fig. 4. (a) Temperature dependent transfer characteristics of the p-GaN gate HEMT with Schottky gate contact in bi-directional measurements. (b) Log-to-log fits between drain current and temperatures.

Fig. 5. (a) Transfer and gate leakage characteristics, (b) temperature dependent transfer characteristics in bi-directional measurements, of the p-GaN gate HEMT with ohmic-type gate contact.

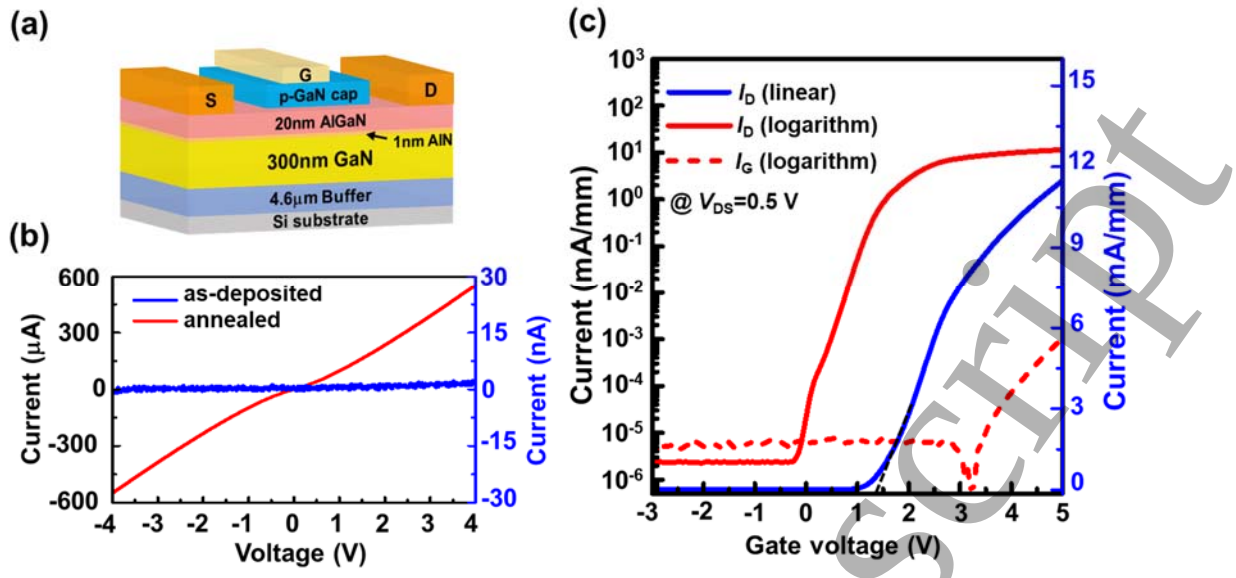

Fig. 1

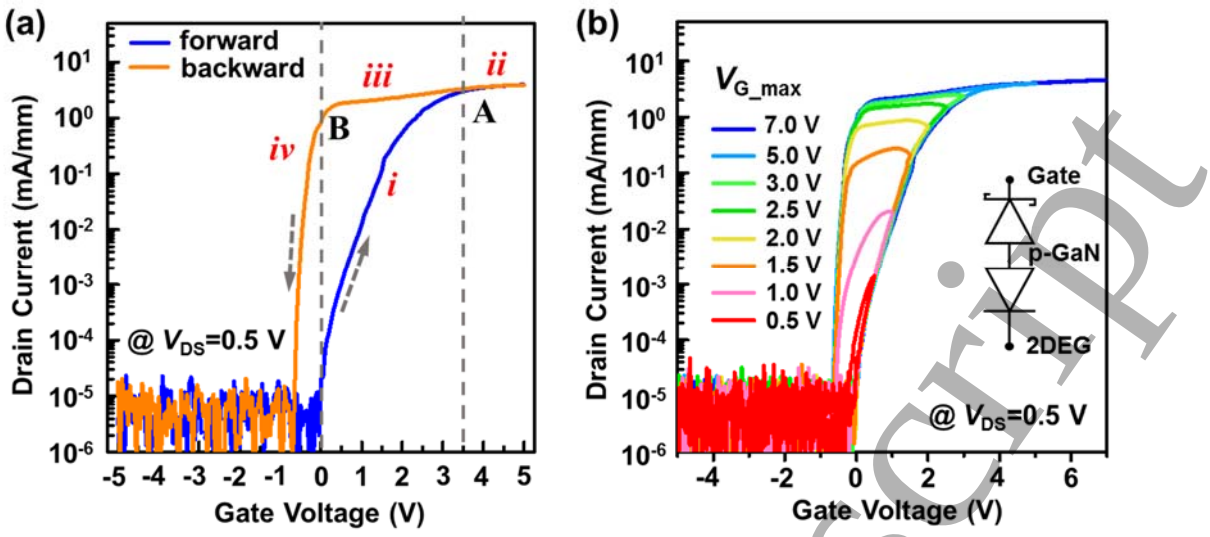

Fig. 2

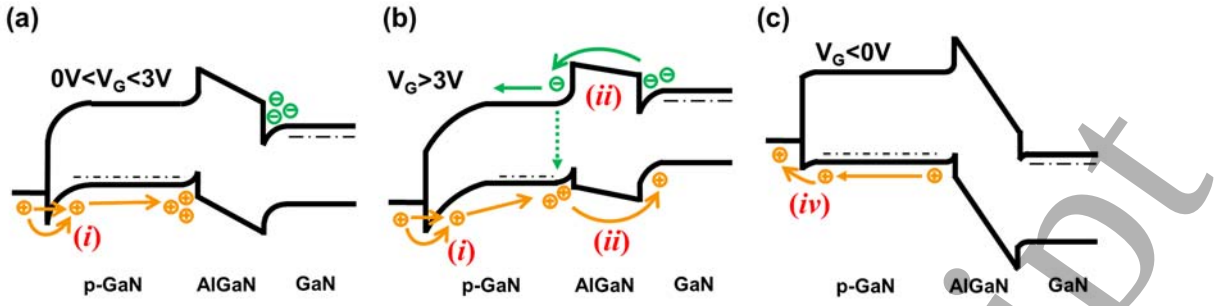

Fig. 3

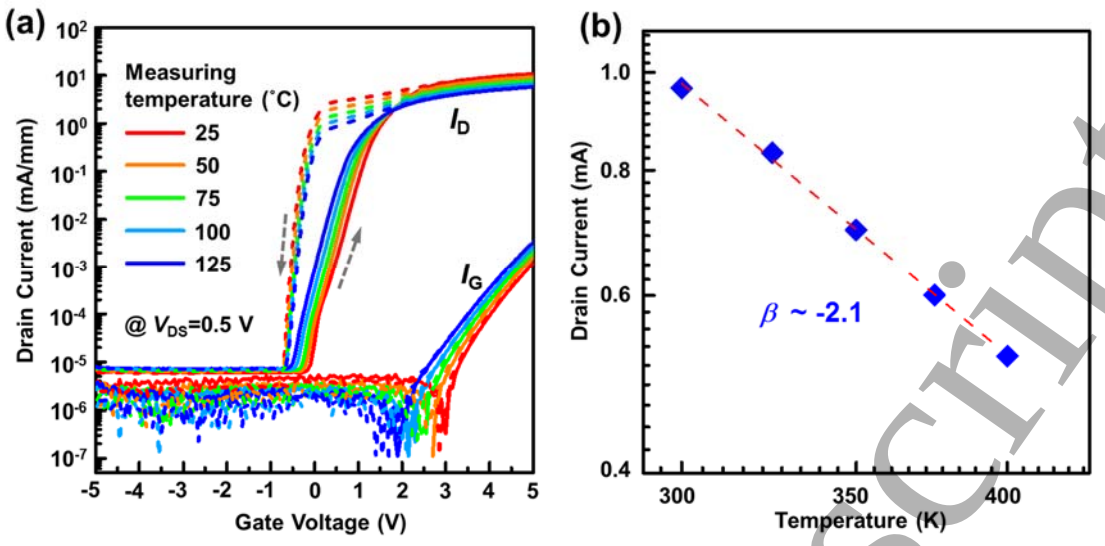

Fig. 4

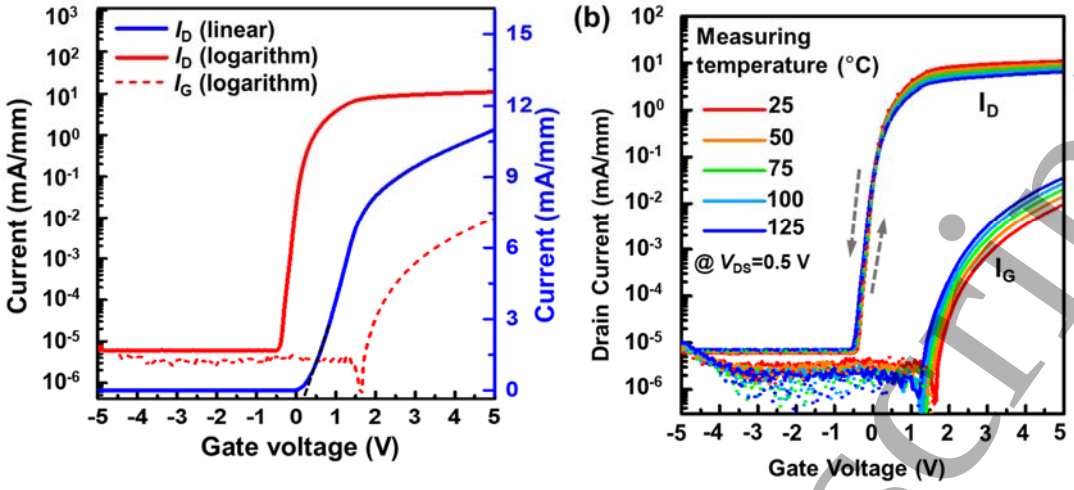

Fig. 5